ON-DIE TERMINATION CIRCUIT AND METHOD FOR REDUCING ON-CHIP DC CURRENT, AND MEMORY SYSTEM INCLUDING MEMORY DEVICE HAVING THE SAME

ABSTRACT OF THE DISCLOSURE

Provided are an on-die termination ("ODT") circuit and ODT method which are capable of minimizing consumption of an on-chip DC current, and a memory system which adopts a memory device having the same, where the ODT circuit includes a termination voltage port, a data input/output ("I/O") port, a first termination resistor, a switch, and a termination enable signal generating circuit; the termination voltage port receives termination voltage from a voltage regulator or a memory controller which is installed outside the memory device; one end of the first termination resistor is connected to the data I/O port; the switch selectively connects the termination voltage port to the other end of the first termination resistor in response to a termination enable signal; the termination enable signal generating circuit generates the termination enable signal in response to a signal which indicates a valid section of input data or that the present period is not a read period during write operations of the memory device, and may also generate the termination enable signal in response to a signal output from a mode register set ("MRS"); and the ODT circuit may include a second termination resistor, one end of which is connected to the data I/O port and the other end of which is connected to the termination voltage port.